AMENDMENT TO THE SPECIFICATION

Please replace paragraph [0008] at page 3, with the following rewritten paragraph:

[0008] In the example of Figure 1, which is an N channel device (a P channel device could also be used with the invention), an N^+ silicon body or other substrate 12 is provided as usual, which conventionally receives a conductive drain electrode 13. An epitixially grown N^- layer 14 is conventionally grown atop substrate 12, for receiving the device junctions. The thickness and resistivity of the layer 14 is determined by the reverse voltage to be withstood by the device and are selected as well known. The active area in Figure 1 contains a well known structure of plural spaced P type base (or channel) diffusion stripes 15, 16 (which could be closed cells, or elements of a trench structure). The channel diffusions 15 and 16 contain conventional N^+ source regions 17 and 18 respectively. The invertible channels between the ends of the N^+ sources 17 and 18 and the ends of base regions 15 and 16 are covered by a conventional MOSgate structure comprising thin gate oxide layers 19, 20, 21 and polysilicon gate electrodes 22, 23 and ~~14~~ 24 respectively. The polysilicon gate electrodes are then insulated as by LTO insulation oxide as usual, and a source electrode 30 is formed on the top surface of the active area.